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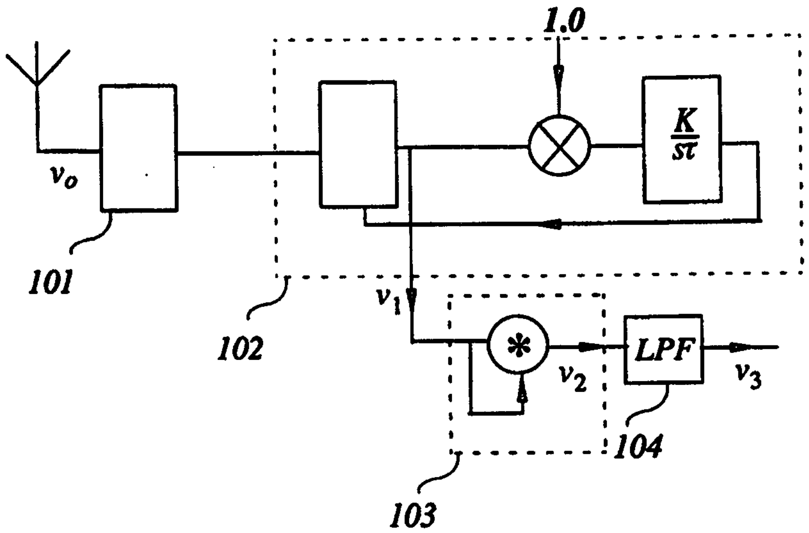
(54) Title: ELECTRONIC CIRCUITS

(57) Abstract

There is described a method and apparatus for separating two independently modulated co–channel interfering fm carriers. The method involves generating a numerator signal being a function of generating a numerator function and a denominator function, the numerator and denominator functions being themselves functions of the ratio of the interfering carrier to the wanted carrier and of the instantaneous difference between the frequency of the wanted carrier and the interfering carrier, and performing a division process between said denominator function and said numerator function to generate a quotient function and using said quotient function to condition an output circuit.



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"Electronic Circuits"

This invention relates to electronic circuits and more particularly to the demodulation of frequency modulated (fm) radio signals.

Whereas electronic circuits for the demodulation of fm signals have been known since the use of fm for radio broadcasting began in the nineteen thirties, there has been a major problem with all existing demodulators, namely, that if two fm transmissions reach the receiver at the same carrier frequency and amplitude, mutual destruction of both transmissions occurs and all intelligibility is lost.

This is a fundamental property of fm demodulators which use saturating circuits prior to the fm demodulator to remove amplitude noise effects from disturbing the wanted signal.

This effect is called co-channel interference especially when the second interfering transmission is a different station. There are four other types of similar interference which result in complete loss of signal.

The first type is called multipath transmission when a delayed version of the same signal is received at the antenna.

The second type is called quasi-sync transmission when the same message is being transmitted on the same frequency but from another transmitter location. At the overlap of the reception, all intelligibility is lost.

The third type is called self-jamming or deliberate-jamming when an unmodulated carrier is transmitted at equal amplitude to the desired modulated carrier. This commonly occurs in military circumstances including laser Dopplerimetry.

The fourth type is called the threshold condition, when the signal is very weak relative to general noise levels. There is a disproportionate increase in demodulated noise levels which causes loss of intelligibility.

These problems exist for all of fm transmissions whether in an analogue or digital format and include spread spectrum technologies.

Demodulation techniques are known which mitigate the first and second types of interference, ie multipath and quasi-sync. In these circuits, the output is the sum of the two carriers and there is no requirement to separate the two carriers since the same information is carried by them both. However, these known techniques are not suitable for separating a pair of independently modulated co-channel interfering carriers, that is, two carriers of similar strength (1-15dB difference) and having the same or similar carrier frequency.

It is an object of the present invention to provide a method and apparatus for minimising and, in some cases, eliminating the aforementioned problems from fm demodulators.

According to the present invention there is provided a method for the demodulation of fm signals, the fm signals comprising a wanted carrier signal and an interfering carrier signal, the method comprising the steps of :- generating a first signal, said first signal being a function of the ratio of the interfering carrier to the wanted carrier and of the instantaneous difference between the frequency of the wanted carrier and the interfering carrier; generating a second signal from said first signal by removing any dc value from said first signal; generating the mathematical square of said second signal; generating a dc value from said squared signal; generating a numerator function being a function of said dc value, said second signal and a dc offset; generating a denominator function being a function of said first signal and said dc offset; performing a division process between said numerator function and said denominator function to generate a quotient function; and using said quotient function to control a demodulator circuit to generate a desired output.

Further according to the present invention there is provided a circuit for demodulating fm signals, the fm signals comprising a wanted carrier signal and an interfering carrier signal, the circuit comprising means for generating a first signal, said first signal being a function of the ratio of the interfering carrier to the wanted carrier and of the instantaneous difference between the frequency of the wanted carrier and the interfering carrier; means for generating a second signal from said first signal by removing any dc value from said first signal; a squaring circuit for generating the mathematical square of said second signal; means for generating a dc value from said squared signal means for generating a numerator function being a function of said dc value, said second signal and a dc offset; means for generating a denominator function being a function of said first signal and said dc offset; a division circuit for performing a division process between said numerator function and said denominator function to generate a quotient function; and a demodulator circuit conditioned by said quotient function to generate a desired output.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Fig. 1 is a block diagram of the initial stage of the circuit of the invention;
Fig. 2 is a block diagram of the denominator function generator stage;
Fig. 3 is a block diagram of the numerator function generator stage;
Fig. 4 are waveforms of the different signals of the block diagrams of Figs 1 to 3;
Fig. 5 is a block diagram of the amplitude-locked loop (ALL) circuit for generating the quotient function of the invention;
Fig. 6 are waveforms of the signals of the circuit of Fig. 5.
Fig. 7 is a block diagram of a phase-locked loop

used in the circuit of the invention;

Fig. 8 is a block diagram illustrating the dominant and sub-dominant channels of the circuit of the invention; and

Figs 9, 10 and 11 illustrate waveforms of the circuit of Fig. 8.

Referring to Fig. 1, a raw received co-channel carrier v_o is passed through a r.f./i.f. stage 101 and through an automatic gain control circuit (AGC) 102 to give v_1 which is termed the co-channel carrier.

$$v_o = \sqrt{1 + 2m\cos\omega_d t + m^2}\cos(\omega_c t + \beta\omega_m\cos\omega_m t)$$

where m is the ratio of the interfering carrier to the wanted carrier;

ω_c is the angular frequency of the wanted carrier;

ω_m is the modulation frequency;

ω_d is the difference frequency between the wanted carrier and the interfering carrier; and

β is the depth of modulation.

v_1 is thus $\dfrac{\sqrt{1 + 2m\cos\omega_d t + m^2}}{\sqrt{1 + m^2}}\cos(\omega_c t + \beta\omega_m\cos\omega_m t)$

The co-channel carrier v_1 is passed to a first pure squaring circuit 103 to give v_2 termed the pure squared received co-channel carrier, where

$$v_2 = \frac{1 + 2m\cos\omega_d t + m^2}{1 + m^2}\cos^2(\omega_c t + \beta\omega_m\cos\omega_m t)$$

v_2 is then passed through a low pass filter 104 to give a filtered squared carrier v_3, where

$$v_3 = \frac{1 + 2m\cos\omega_d t + m^2}{1 + m^2}$$

If m′ is defined as $\frac{2m}{1 + m^2}$

then v_3 becomes $1 + m'\cos\omega_d t$

Referring now to Fig. 2, the filtered squared signal v_3 is added to a small dc offset v_7 in adder 108 to give a denominator function, signal v_8,

where $v_8 = 1 + m'\cos\omega_d t + v_{offset}$

Referring to Fig. 3, v_3 is passed to high pass filter 105 to remove the dc content to give v_4, where

$$v_4 = m'\cos\omega_d t$$

v_4 is then passed to a second pure squaring circuit 106 to give v_5, termed the twice squared co-channel carrier, where

$$v_5 = m'^2\cos^2\omega_d t$$

v_5 is passed through low pass filter 107 to give a filtered twice squared signal, where

$$v_6 = m'^2$$

Adder 109 serves to add signal v_6, signal v_4 and subtract the dc offset v_7 to give a numerator function v_9, where

$$v_9 = m'^2 + m'\cos\omega_d t - v_{offset}$$

The main waveforms of the signals appearing in the circuits of Figs 1 to 3 are illustrated in Fig. 4.

The denominator function v_8 from the circuit of Fig. 2 and the numerator function v_9 from the circuit of Fig. 3 are processed as follows, with reference to Fig. 5.

The denominator function v_8 and the numerator function v_9 are processed in an amplitude-locked loop (ALL) circuit 110. The ALL circuit 110 comprises an adder 111, an operational amplifier 112 and a multiplier 113. The output of the ALL 110 is a quotient function v_{10} obtained by dividing the numerator function v_9 by the denominator function v_8, to give

$$v_{10} = \frac{m'^2 + m'\cos\omega_d t - v_{offset}}{1 + m'\cos\omega_d t + v_{offset}}$$

The quotient function v_{10} is passed to an adder 114 to which there is also input a dc signal v_{11}

In a normalised system, the signal v_{11} has a value of 1 volt. v_{10} and v_{11} combine to give a signal v_{12}, where v_{12} is defined as $v_{10}+1$

$$\text{thus } v_{12} = \frac{1 + 2m'\cos\omega_d t + m'^2}{1 + m'\cos\omega_d t + v_{offset}}$$

The main waveforms of the signals appearing in the circuit of Fig. 5 are illustrated in Fig. 6.

The signals v_{10} and v_{12} are used to condition an fm demodulator as illustrated in Fig. 8.

Referring now to Fig. 7, a PLL demodulator 117, the input to which is the stabilised output of the AGC circuit 102 of Fig. 1, that is, the co-channel carrier

v_1, produces an output v_{13} being a combination of the dominant carrier and the subdominant carrier, the dominant being an unmodulated carrier and the subdominant carrier being a modulated carrier.

Output v_{13} can be expressed as

$$v_{13} = \frac{m^2 + m\cos\omega_d t}{(1 + 2m\cos\omega_d t + m^2)}\beta\omega_m \cos\omega_m t$$

Referring now to Fig. 8, the fm demodulator comprises a subdominant channel 121 and a dominant channel 122.

The subdominant channel 121 comprises a multiplier 123 fed by signal v_{10} and signal v_{13}. The output of the multiplier 123 (signal v_{14}) is fed through a low pass filter 125 to give a signal v_{15} being the recovered sub-dominant signal which is passed to a level conditioner 127 which has a second input being the filtered twice-squared carrier signal v_6. The output of the level conditioner 127 is sub-dominant signal v_{16} free of any crosstalk of the dominant carrier, and restored to its normal value.

The waveforms for the sub-dominant channel 121 are shown in Fig. 9, when the sub-dominant, wanted signal is modulated.

In the case where the dominant, unwanted, signal is modulated, as illustrated in Fig. 10, waveform v_{23} multiplied by signal v_{10} results in suppression of the dominant signal, as illustrated in waveform v_{25}.

The dominant channel 122 comprises a multiplier 124 fed by signal v_{12} and signal v_{13} to give output v_{17}. The output of multiplier 124 (v_{17}) is fed to adder 128 through low pass filter 126. A second input to the adder 128 is the signal v_{15} from low pass filter 125 in the subdominant channel 121. The output of the adder 128 is thus the dominant carrier free of any crosstalk from the subdominant carrier. The waveforms for the dominant channel are shown in Fig. 11.

Thus the circuit has two distinct outputs. The first, v_{16}, is the recovered subdominant free of any dominant carrier content, and the second, v_{19}, is the recovered dominant carrier free of any sub-dominant content.

The circuits of the invention thus provide for the separation of two independently modulated co-channel interfering carrier of similar strength and having the same or similar carrier frequency.

CLAIMS

1 A method for the demodulation of fm signals, the fm signals comprising a wanted carrier signal and an interfering carrier signal, the method comprising the steps of :- generating a first signal (v_3), said first signal (v_3) being a function of the ratio (m) of the interfering carrier to the wanted carrier and of the instantaneous difference (ω_d) between the frequency of the wanted carrier and the interfering carrier; generating a second signal (v_4) from said first signal (v_3) by removing any dc value from said first signal (v_3); generating the mathematical square (v_5) of said second signal (v_4); generating a dc value (v_6) from said squared signal (v_5); generating a numerator function (v_9) being a function of said dc value (v_6), said second signal (v_4) and a dc offset (v_7); generating a denominator function (v_8) being a function of said first signal (v_3) and said dc offset (v_7); performing a division process between said numerator function (v_9) and said denominator function (v_8) to generate a quotient function (v_{10}); and using said quotient function (v_{10}) to control a demodulator circuit to generate a desired output.

2 A method as claimed in Claim 1 wherein said first signal (v_3) is generated by squaring an initial signal (v_1) to give a squared initial signal (v_2), and passing said squared initial signal (v_2) through a low pass filter (104).

3 A method as claimed in Claim 2 wherein said initial signal (v_1) is derived by passing an input co-channel carrier (v_0) through an automatic gain control circuit (102).

4 A method as claimed in any preceding Claim wherein

said quotient function (v_{10}) is generated by dividing said numerator function (v_9) by said denominator function (v_8) in an Amplitude Locked Loop circuit (110).

5 A method as claimed in either Claim 3 or Claim 4 including the step of generating, from said initial signal (v_1), a demodulated output signal (v_{13}) by passing said initial signal (v_1) through a Phase Locked Loop circuit (102).

6 A method as claimed in Claim 5 including the step of multiplying said quotient function (v_{10}) with said demodulated output signal (v_{13}) to generate a first intermediate output (v_{14}).

7 A method as claimed in Claim 6, including the step of passing said first intermediate output (v_{14}) through a low pass filter (125) to generate a first filtered output (v_{15}).

8 A method as claimed in Claim 7, including the step of multiplying said first filtered output (v_{15}) by said dc value (v_6) to give a first desired output (v_{16}).

9 A method as claimed in any preceding claim, including the step of adding a dc voltage (v_{11}) to the said quotient function (v_{10}) to generate a modified quotient function (v_{12}).

10 A method as claimed in any one of Claims 5 to 9, including the step of multiplying said modified quotient signal (v_{12}) by said demodulated output (v_{13}) to give a second intermediate output (v_{17}).

11 A method as claimed in Claim 10, including passing said second intermediate output (v_{17}) through a low pass filter (126) to give a second filtered output (v_{18}) and

subtracting from said second filtered output (v_{18}) said first filtered output (v_{15}) to give a second desired output (v_{19}).

12 A circuit for demodulating FM signals, the FM signals comprising a wanted carrier signal and an interfering carrier signal, the circuit comprising means (102, 103,104) for generating a first signal (v_3), said first signal (v_3) being a function of the ratio (m) of the interfering carrier to the wanted carrier and of the instantaneous difference (ω_d) between the frequency of the wanted carrier and the interfering carrier; means (105) for generating a second signal (v_4) from said first signal (v_3) by removing any dc value from said first signal (v_3); a squaring circuit (106) for generating the mathematical square (v_5) of said second signal (v_4); means (107) for generating a dc value (v_6) from said squared signal (v_5); means (109) for generating a numerator function (v_9) being a function of said dc value (v_6), said second signal (v_4) and a dc offset (v_7); means (108) for generating a denominator function (v_8) being a function of said first signal (v_3) and said dc offset (v_7); a division circuit (110) for performing a division process between said numerator function (v_9) and said denominator function (v_8) to generate a quotient function (v_{10}); and a demodulator circuit (120) conditioned by said quotient function (v_{10}) to generate a desired output.

13 A circuit as claimed in Claim 12, wherein said means for generating said second signal (v_4) from said first signal (v_3) is a high pass filter (105).

14 A circuit as claimed in either of Claims 12 or 13, wherein said means for generating said dc value (v_6) is a low pass filter (107).

15 A circuit as claimed in any one of Claims 12 to 14, wherein said means for generating said numerator function (v_9) is an adder circuit (109).

16 A circuit as claimed in any one of Claims 12 to 15, wherein said means for generating said numerator function (v_8) is an adder circuit (108).

17 A circuit as claimed in any of Claims 12 to 17, wherein said division circuit (110) is an Amplitude Locked Loop Circuit.

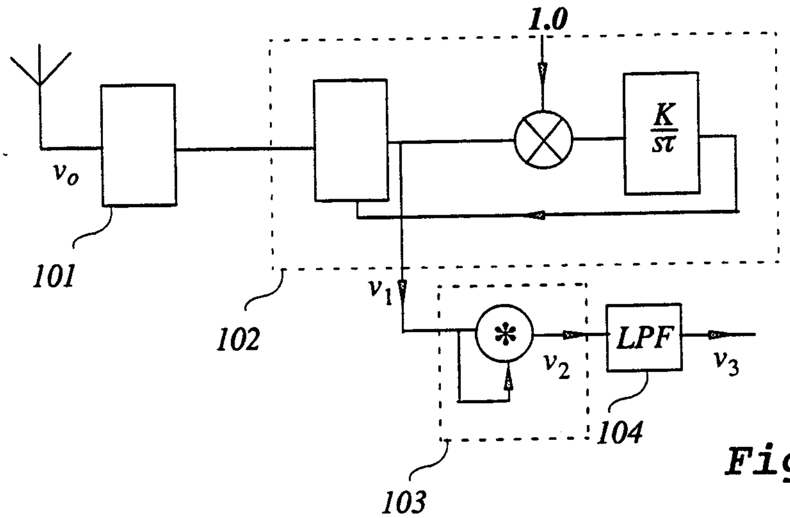


Fig 1

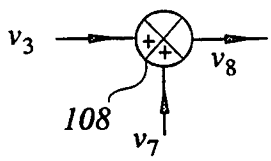


Fig 2

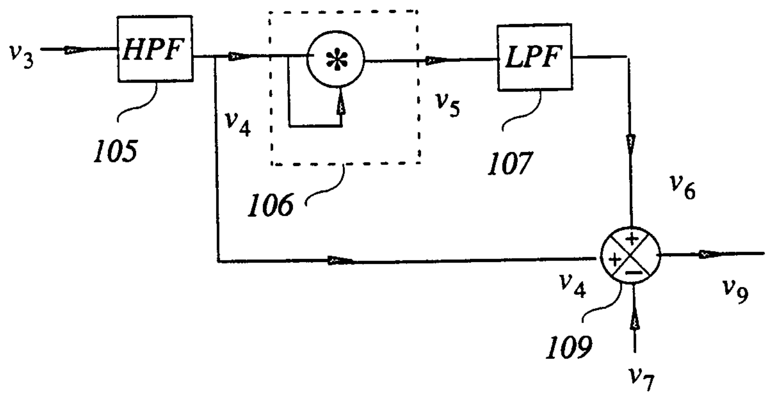


Fig 3

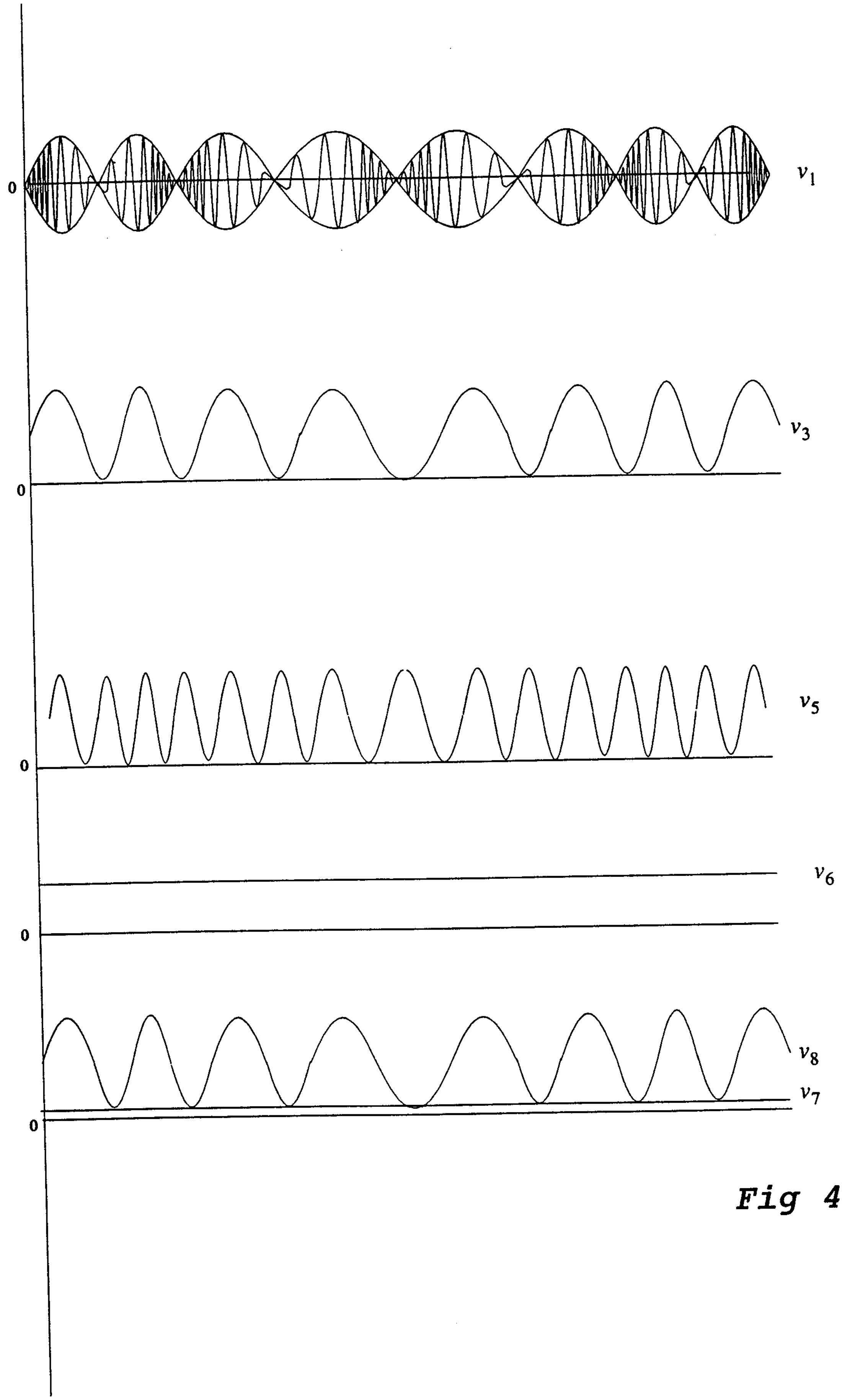


Fig 4

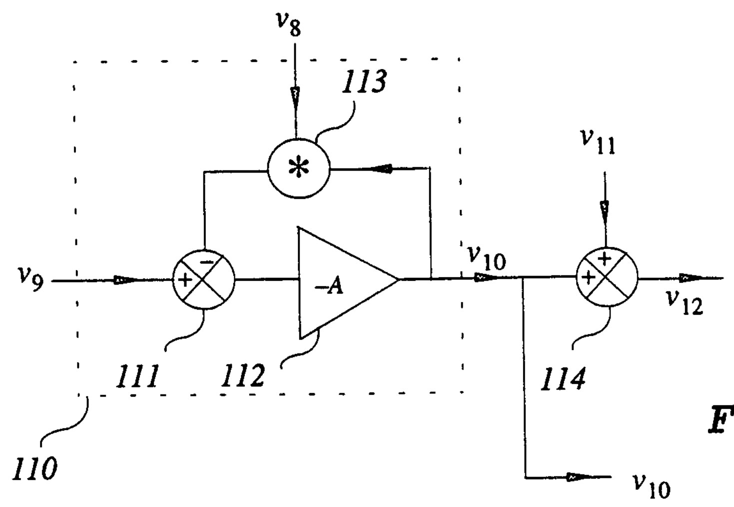


Fig 5

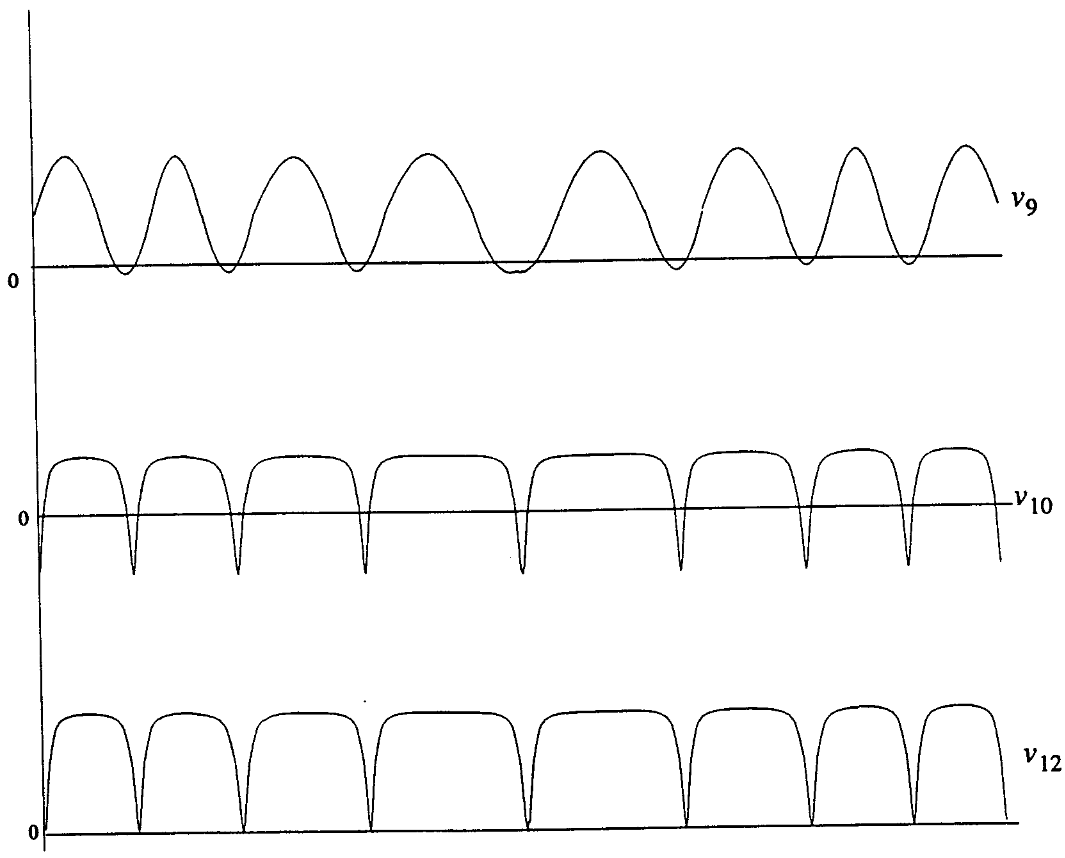
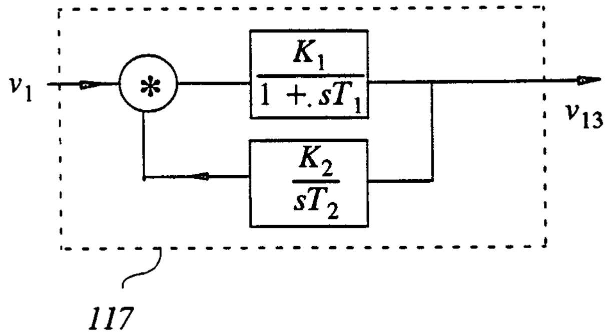
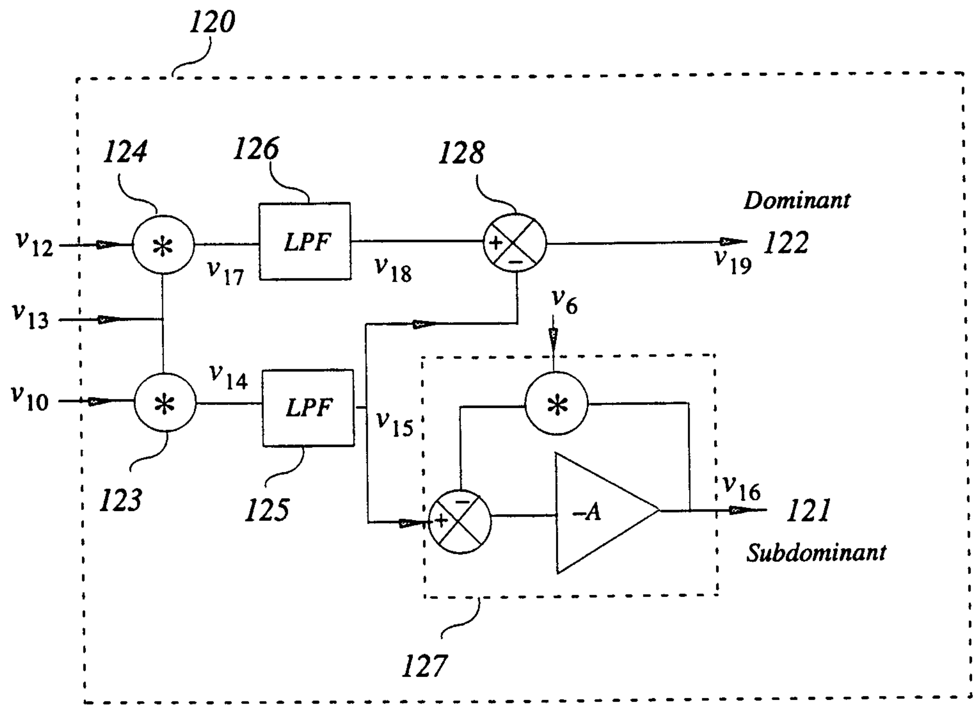


Fig 6



v_1
*
$\frac{K_1}{1+.sT_1}$
$\frac{K_2}{sT_2}$
v_{13}
117

Fig 7



120
124
126
128
Dominant
v_{12}
*
LPF
v_{17}
v_{18}
v_{19}
122
v_{13}
v_6
v_{10}
v_{14}
LPF
v_{15}
*
v_{16}
121
–A
Subdominant
123
125
127

Fig 8

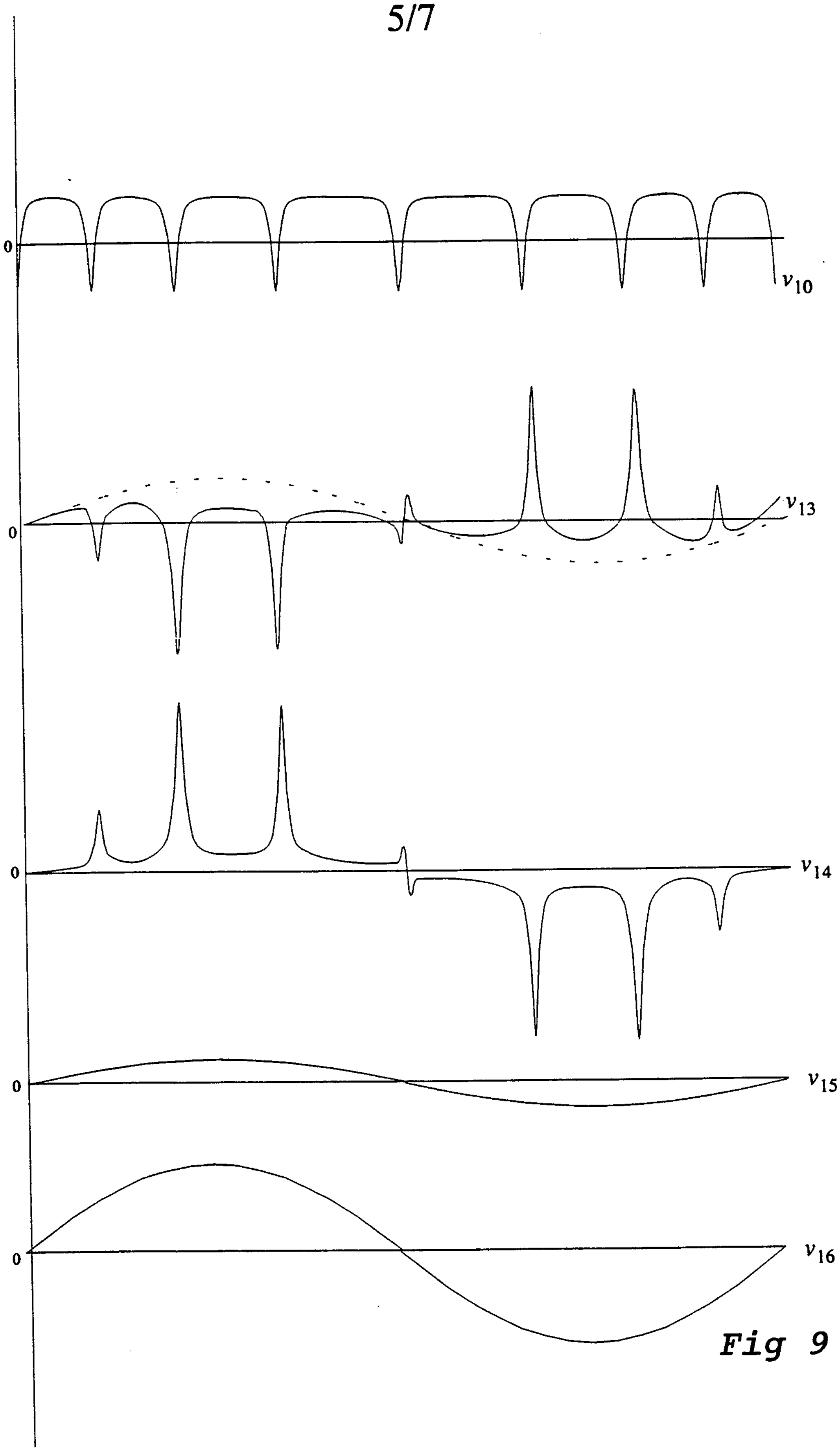


Fig 9

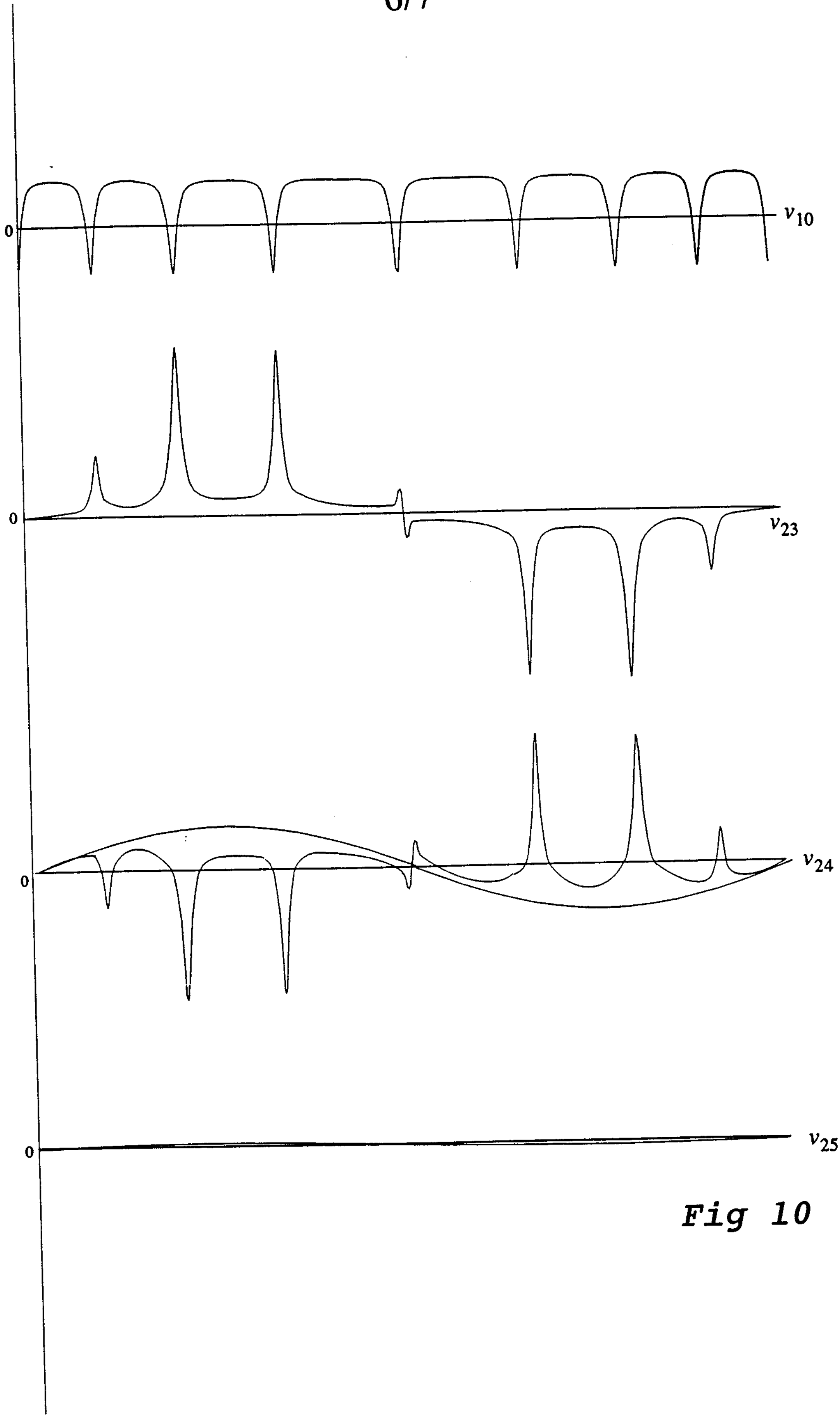


Fig 10

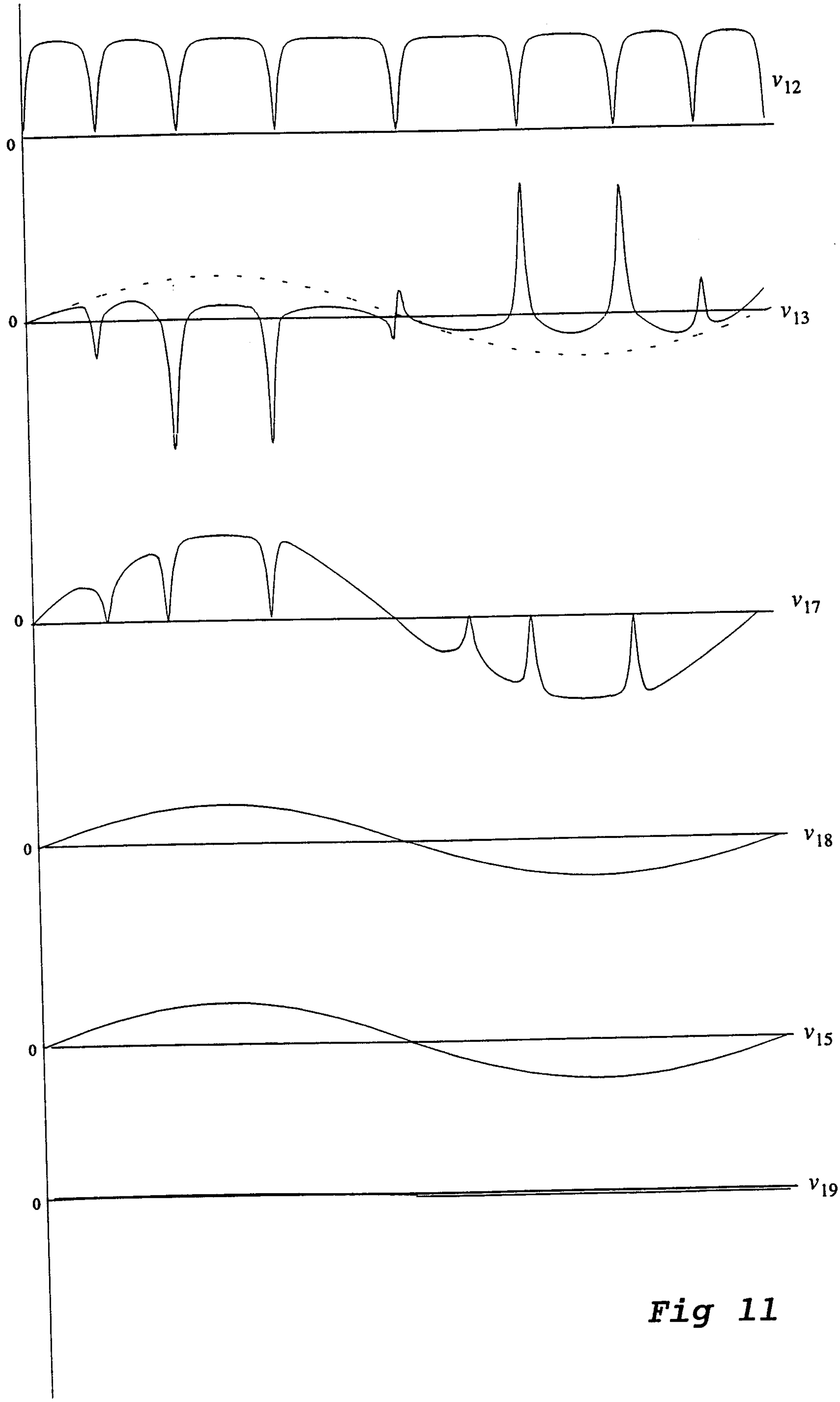


Fig 11

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/00629

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03D3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03D H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PETTIGREW A: "DEMODULATION A NEW APPROACH" ELECTRONICS WORLD AND WIRELESS WORLD, vol. 101, no. 1717, 1 December 1995, pages 1026-1031, XP000548985 see page 1030, column 2, line 29 - page 1031, column 3, line 6; figure 8	1,12
A	PATENT ABSTRACTS OF JAPAN vol. 005, no. 179 (E-082), 17 November 1981 & JP 56 106434 A (SONY CORP), 24 August 1981 see abstract	1,12
A	US 5 341 106 A (PETTIGREW ARCHIBALD M) 23 August 1994 see abstract; figures 12,21A	1,12

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
18 June 1999	25/06/1999

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	WO 97 20397 A (NORTHERN TELECOM LTD) 5 June 1997 see page 1, line 26 - page 8, line 29; figures 2,4,5 ---	1,12
A	PETTIGREW A M ET AL: "COHERENT DEMODULATION OF DSSC WITHOUT PILOT TONE USING THE AMPLITUDE-LOCKED LOOP" JOURNAL OF THE AUDIO ENGINEERING SOCIETY, vol. 41, no. 12, 1 December 1993, pages 998-1007, XP000514962 -----	

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
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